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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,074	07/14/2003	Pradip Patel	03-0580/LSI1P226	7110

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,074	PATEL ET AL.	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *10-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 16-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/620074 Attorney's Docket #: 03-0580 (LSI1P226)
Filing Date: 7/14/2003;

Applicant: Patel et al.

Examiner: Alexander Williams

Applicant's election with traverse of Group I (claims 1 to 9 and 16 to 18), filed 4/6/04, has been acknowledged.

Applicant's arguments in response to the restriction has been considered.

Inventions I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the device can operate with a different system. The subcombination has separate utility such as being an IC semiconductor IC package.

In the examination of claims Group I (claims 1 to 9 and 16-18) the Examiner would be interested in searching for the final structure of the semiconductor device claimed. In the examination of Group II (claims 10-15) the Examiner would be interested in multiple components to perform the system claimed. Therefore, the two Groups would require a search in different art units and class. The Examiner would not be unduly burdened to evaluate all claims fully on their merit at the full time.

Each of the Groups have searches in different art units and classes that would unduly burden the Examiner to evaluate all claims on their merit at the full time. This is not found persuasive because of the reasons detailed in the last Office action.

The requirement is still deemed proper and is therefore made FINAL.

This application contains claims 10-15 drawn to an invention non-elected with traverse. A complete response to the final rejection must include cancellation of non-elected claims or other appropriate action (see 37 CFR § 1.144 & MPEP § 821.01).

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the flip chip package, in claim 7 and 9 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to because the cross-sectional views in the drawings are not correctly or acceptably cross hatched. Without the correct cross-hatched views, the drawings are confusing and not easy to comprehend without a direct layer-for-layer association with the specification. Applicant is directed to MPEP § 608.02 and specifically, the table at page 600-51 (Rev 14, Nov. 1992) of the MPEP for help in correcting the drawings.

Correction is required.

Claims 2 to 5, 7 to 9 and 16 to 18 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, line 3, "at least one electrical ground plane" should probably be –the at least one electrical ground plane--.

In claim 3, line 2, "the ground plane" should be consistent with the –the at least one electrical ground plane--.

In claim 5, line 3, "mounting pegs, and thermal solder balls" should probably be – the conductive mounting pegs, and the thermal solder balls--.

In claims 7 and 9, it is unclear and confusing to what is meant by and what shows "the flip chip package."

In claim 16, it is unclear and confusing to what is meant by and what shows "a substrate including **at least one electrical ground plane** and having a plurality solder balls formed on a surface thereof, said solder balls including a set of thermal solder balls electrically connected with **a ground plane** and positioned near the perimeter of the package." Are the at least one electrical ground plane and a ground plane the same?

In claim 18, it is unclear and confusing to what is meant by and what shows "An electronic device incorporating the IC package of Claim 16 wherein the electronic device comprises a computer device."

Any of claims 2 to 5, 7 to 9 and 16 to18 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 6, 8 and 16 to 18, **insofar as some of them can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Zhong et al. (U.S. Patent Application Publication # 2003/0179549 A1).

1. Zhong et al. (figures 2A to 15B) specifically figures 7A and 7F show a semiconductor integrated circuit (IC) package **700** comprising:
a substrate **302** including at least one electrical ground plane **720** and having a plurality solder balls **306** formed on a surface thereof, said solder balls including a set of thermal solder balls positioned near the perimeter of the package;
an integrated circuit die **304,704** mounted to the substrate such that the die is electrically connected with some of the solder balls; and
a heat spreader **706** mounted on the package such that the heat spreader is in thermal communication with the die and also in thermal communication with the set of thermal solder balls positioned near the perimeter of the package thereby enabling a portion of the heat generated by the die to be dissipated from the die through the heat spreader into the set of thermal solder balls.

2. The IC package of Claim 1, Huang et al. show wherein the set of thermal solder balls **306** is electrically connected to said at least one electrical ground plane **720**; and wherein the heat spreader, at least one electrical ground plane, and the set of thermal solder balls are arranged so that heat generated by the die can be dissipated from the die through the heat spreader into the at least one electrical ground plane and into the set of thermal solder balls.

3. The IC package of Claim 2, Zhong et al. show wherein the heat spreader **706** electrically connected to the ground plane **720** operates to reduce electrical noise generated by the package.

4. The IC package of Claim 3, Zhong et al. show wherein the heat spreader **706** is connected to the thermal solder balls **306** using conductive mounting pegs **314** and wherein the heat spreader forms part of a electromagnetic shield that reduces the overall electrical noise generated by the package.

5. The IC package of Claim 3, Zhong et al. show wherein the heat spreader **706** is connected to the thermal solder balls **306** using conductive mounting pegs **314** and wherein the heat spreader, mounting pegs, and thermal solder balls form, in combination, part of a electromagnetic shield that reduces the overall electrical noised generated by the package.

16. Zhong et al. (figures 2A to 15B) specifically figures 7A and 7F show a semiconductor integrated circuit (IC) package **700** comprising:
a substrate **302** including at least one electrical ground plane **720** and having a plurality solder balls **306** formed on a surface thereof, said solder balls including a set of thermal solder balls electrically connected with a ground plane and positioned near the perimeter of the package,
an integrated circuit die **304,704** mounted to the substrate such that the die is electrically connected with some of the solder balls;
a heat spreader **706** mounted on the package with conductive mounting pegs **314** that are electrically connected with the ground plane and such that the heat spreader is in thermal communication with the die and in thermal communication with the set of thermal solder balls thereby enabling a portion of the heat generated by the die to be dissipated from the die through the heat spreader into the set of thermal solder balls; and
the combination of the electrically connected heat spreader, ground plane, and conductive mounting pegs operating together as a electromagnetic shield that reduces the amount of electrical noise of the package.
17. Zhong et al. show an electronic device incorporating the IC package of Claim 16.

Claims 1 to 3, 6 and 8, **insofar as some of them can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Huang et al. (U.S. Patent # 6,703,698 B2).
1. Huang et al. (figures 1A to 2E) specifically figure 2E show a semiconductor integrated circuit (IC) package comprising:
a substrate **200** including at least one electrical ground plane **201b** and having a plurality solder balls **260** formed on a surface thereof, said solder balls including a set of thermal solder balls positioned near the perimeter of the package;
an integrated circuit die **210** mounted to the substrate such that the die is electrically connected with some of the solder balls; and
a heat spreader **230,220** mounted on the package such that the heat spreader is in thermal communication with the die and also in thermal communication with the set of thermal solder balls positioned near the perimeter of the package thereby enabling a portion of the heat generated by the die to be dissipated from the die through the heat spreader into the set of thermal solder balls.

2. The IC package of Claim 1, Huang et al. show wherein the set of thermal solder balls **201b,262** is electrically connected to said at least one electrical ground plane **201b**; and wherein the heat spreader, at least one electrical ground plane, and the set of thermal solder balls are arranged so that heat generated by the die can be dissipated from the die through the heat spreader into the at least one electrical ground plane and into the set of thermal solder balls.
3. The IC package of Claim 2, Huang et al. show wherein the heat spreader **232** electrically connected to the ground plane **201b** operates to reduce electrical noise generated by the package.
4. The IC package of Claim 3, Huang et al. show wherein the heat spreader **230** is connected to the thermal solder balls **260** using conductive mounting pegs **201c** and wherein the heat spreader forms part of a electromagnetic shield that reduces the overall electrical noise generated by the package.
5. The IC package of Claim 3, Huang et al. show wherein the heat spreader is connected to the thermal solder balls using conductive mounting pegs and wherein the heat spreader, mounting pegs, and thermal solder balls form, in combination, part of a electromagnetic shield that reduces the overall electrical noised generated by the package.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a ground plane and a conductive mounting pegs deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of

obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Therefore, it would have been obvious to one of ordinary skill in the art to use the ground planes and the conductive mounting pegs as "merely a matter of obvious engineering choice" as set forth in the above case law.

Claims 4, 5 and 16 to 18, **insofar as they can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Huang et al. (U.S. Patent # 6,703,698 B2).

4. The IC package of Claim 3, Huang et al. show wherein the heat spreader **230** is connected to the thermal solder balls **260** using conductive mounting pegs **201c** and wherein the heat spreader forms part of a electromagnetic shield that reduces the overall electrical noise generated by the package.

5. The IC package of Claim 3, Huang et al. show wherein the heat spreader is connected to the thermal solder balls using conductive mounting pegs and wherein the heat spreader, mounting pegs, and thermal solder balls form, in combination, part of a electromagnetic shield that reduces the overall electrical noised generated by the package.

16. Huang et al. (figures 1A to 2E) specifically figure 2E show a semiconductor integrated circuit (IC) package comprising:

a substrate **200** including at least one electrical ground plane **201b** and having a plurality solder balls **260** formed on a surface thereof, said solder balls including a set of thermal solder balls electrically connected with a ground plane **201b** and positioned near the perimeter of the package,

an integrated circuit die **210** mounted to the substrate such that the die is

electrically connected with some of the solder balls;
a heat spreader **230,220** mounted on the package with conductive mounting pegs **201b** that are electrically connected with the ground plane and such that the heat spreader is in thermal communication with the die and in thermal communication with the set of thermal solder balls thereby enabling a portion of the heat generated by the die to be dissipated from the die through the heat spreader into the set of thermal solder balls; and the combination of the electrically connected heat spreader, ground plane, and conductive mounting pegs operating together as a electromagnetic shield that reduces the amount of electrical noise of the package.
17. Huang et al. show an electronic device incorporating the IC package of Claim 16.

Therefore, it would have been obvious to one of ordinary skill in the art to use the ground planes and the conductive mounting pegs as "merely a matter of obvious engineering choice" as set forth in the above case law.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/712,713,717,720,668,778,737,738,734,691,696,698, 675,676,796,784,786,706,707,734	6/4/04
Other Documentation: foreign patents and literature in 257/712,713,717,720,668,778,737,738,734,691,696,698, 675,676,796,784,786,706,707,734	6/4/04
Electronic data base(s): U.S. Patents EAST	6/4/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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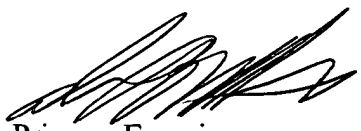

Primary Examiner
Alexander O. Williams